

REMARKS

I. Status of Application

Claims 1-31 are all the claims pending in the application and, of these claims, claims 25-31 have been withdrawn. Claims 1-24 have been rejected.

II. Formalities

The Examiner has acknowledged Applicant's claim to foreign priority and has indicated that all of the certified copies of the priority documents have been received.

The Examiner has indicated that the drawings filed on September 26, 2006 have been accepted.

The Examiner has considered all the references cited with the Information Disclosure Statement filed on September 26, 2006.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 1-7, 9-15 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster (U.S. 6,285,064) in view of Herndon et al (U.S. 6,444,076), Lee (U.S. 6,660,562), Hayasaka et al (U.S. 7,089,986), Amo (U.S. 6,200,402), and Kato et al (U.S. 4,275,306). Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster, in view of Herndon, Lee, Hayasaka, Amo, and Kato, as applied to claim 1 above, and further in view of Murakami et al (U.S. 4,248,750). Claims 16, 18-21, and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of Herndon, Lee, Hayasaka, Amo, and Kato, as applied to claims 1 and 11 above, and further in view of Yoshikawa (U.S. 4,752,180). Claim 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster, in view of Herndon, Lee, Hayasaka, Amo, Kato, and Yoshikawa, as applied to claim 21 above, and further in view of Koyanagi et al

(JP 05-160340 A). Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster, in view of Herndon, Lee, Hayasaka, Amo, and Kato, as applied to claim 1 above, and further in view of Glennon (U.S. 4,243,500). Applicant respectfully traverses all of these rejections.

Independent claim 1 recites (among other things):

...a parallelism adjusting section for
adjusting parallelism of said joint surface of
said semiconductor substrate and said joint
surface of said sealing substrate on which said
adhesive layer is formed...

The cited references, and any combination thereof, fail to teach or suggest these features and, therefore, claim 1 is patentable over the cited references for *at least* these reasons.

The Examiner acknowledges that Foster, Herndon, Lee, Hayasaka, Amo, and any combination thereof, fails to teach or suggest the above features (05/27/09 Office Action, page 7). Nevertheless, the grounds of rejection allege that Kato teaches a parallelism adjusting section, as claimed. Applicant respectfully disagrees with the grounds of rejection and submits that Kato fails to teach or suggest a parallelism adjusting section for adjusting parallelism of a joint surface of a semiconductor substrate (e.g., a wafer) and a joint surface of a sealing substrate (e.g., cover glass), as recited in claim 1.

In contrast to claim 1, Kato discloses a device for producing a semiconductor circuit element by transferring a circuit pattern formed on the mask 12 to the wafer 13 (Fig. 1, laser light source 1 to wafer 13, col. 2, lines 41-54, col. 1, lines 12-15). Kato teaches that the wafer 13 is supported by a wafer carrier which is parallel-movable in the directions x , y , and θ by pulse motors. One of ordinary skill in the art would readily discern from Kato that the reason for parallelizing a masking surface with a wafer surface by aligning the mask 12 and the wafer 13 in

accordance with respective alignment marks thereon, is to make a circuit pattern accurately exposed on the wafer surface through the mask (*see e.g.*, FIG. 1, laser source 1, wafer 13, light path in Fig. 1).

Therefore, while Kato may teach that the wafer 13 is supported by a wafer carrier that is parallel-movable, it is not necessary for Kato's device to join the wafer 13 and the mask 12. Since Kato's mask 12 is not joined with the wafer 13, Kato's mask 12 does not correspond to a sealing substrate for individually sealing plural elements formed on a semiconductor substrate, as recited in claim 1. Further, Kato does not teach, and cannot possibly suggest, the features of said joint surface of said semiconductor substrate, or said joint surface of said sealing substrate, as claimed. Indeed, Kato does not mention any joint surfaces at all. Applicant respectfully submits that because the cited references fail to teach or suggest all the recitations of claim 1, claim 1 would not have been obvious in view of the cited references for *at least* these reasons.

Additionally, there would have been no reason for one of ordinary skill in the art to modify the teachings of Foster with those of Kato so as to arrive at the recitations of claim 1. For instance, it is not necessary for Kato's device to adjust the parallelism of the joint surface of a semiconductor substrate and the joint surface of the sealing substrate. Consequently, there would have been no reason for one of ordinary skill in the art to apply the teachings of Kato to those of Foster, which is directed to joining a cover glass to a wafer, so as to achieve the recitations of claim 1.

Thus, claim 1 would not have been obvious in view of the cited references for *at least* these additional independent reasons. Moreover, the dependent claims 2-24 are patentable over the cited references *at least* by virtue of their dependency on claim 1.

In addition, with respect to claim 11, even assuming *arguendo* that one of ordinary skill in the art would have looked to Kato so as to modify Foster's teachings by adjusting the parallelism of Foster's cover glass and wafer, Kato nevertheless fails to teach or suggest the features of a section for measuring clearances between said joint surface of said semiconductor substrate and said joint surface of said sealing substrate at plural measurement points, as claimed.

In sharp contrast to claim 11, Kato teaches moving the wafer 13 and the mask 12 along x , y and θ directions while maintaining the parallelism of the wafer 13 and the mask 12 (col. 2, lines 32-34). However, Kato's x , y and θ directions are not related to clearances between the surface of the wafer 13 and the surface of the mask 12. Indeed, Kato teaches that these x , y and θ directions are merely changed to alter the directions of the wafer 13 and the mask 12 so as to align the alignment marks thereon while the parallelism of the wafer surface and the masking surface is maintained (col. 3, line 55- col. 4, line 33).

Specifically, FIGS. 3-5 of Kato show alignment marks (reference numerals 30-39) (col. 2, lines 8-13). In view of the arrow signs represented by "x" and "y" in FIG. 5, it is clear from Kato that the x -axis and the y -axis directions are parallel with respect to the wafer and the mask surfaces. Kato does not explicitly define the parameter θ , however, one of ordinary skill in the art would have recognized that the parameter θ references some rotational direction on the surface represented by the x -axis and the y -axis directions and does not reference clearances between the surface of the wafer 13 and the surface of the mask 12. This is because (among other reasons): (1) according to Kato's teachings, and as shown particularly in FIG. 1, maintaining the parallelism of the wafer 13 surface and the mask 12 surface is necessary for making an accurately exposed circuit pattern on the wafer 13 with mask 12, and also (2) the

rotational amount (H) of θ is represented only by Δy (col. 4, lines 22-28 and lines 61-65; equation (5)).

Accordingly, even assuming *arguendo* that Kato discloses maintaining the parallelism of the wafer surface and the masking surface, Kato is not related with clearances between the wafer surface and the masking surface. Thus, Kato does not teach or suggest measuring clearances between the wafer surface and the masking surface at plural measurement points, as required by claim 11. Therefore, Applicant respectfully submits that claim 11 is patentable over the cited references for *at least* these additional reasons.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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